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A Temperature Compensated CMOS Differential Ring Oscillator with Low Power Consumption for RFID Applications

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A b s t r a c t

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This paper presents the three-delay-stage low power differential ring oscillator used for RFID applications. To make oscillator frequency independent from temperature, two temperature compensation methods have been used. In the first method the NMOS diode-connected transistor is connected in series with PMOS load. As a result of complementary behavior of NMOS and PMOS, the temperature variation of the output voltage is reduced at each stage. In the second method in order to decrease the dependence of oscillator current to temperature, a diode-connected transistor has been used in the current supply. The simulation is done by cadence software in 0.18 µm CMOS technology, and the power consumption of oscillator is 502 nW. At the central frequency of 7 MHz, the frequency deviation within the temperature range of -10 to 150°C is equal to 267 ppm/°C. Also the phase noise of the oscillator at the offset frequency of 100 KHz is -80.2 dBc/Hz, and the jitter period for 10000 cycles is 0.94 ns (rms).

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1. Introduction

An RFID system is the radio frequency identification system which consists of at least a reader and a tag. Regarding to the increasing advancement and needs of industry for more accurate and easier identification of products, great improvement has been made in RFID systems in order to reduce the cost and to fabricate it more comfortably.

To reduce the cost, the UHF RFID passive tags are used. No battery is implemented on the tag chips, so they supply their energy from the waves transmitted by the reader, and to respond the reader, they work according to the backscattering received signal. Regarding to Figure 1 the RFID passive tag consists of four blocks: analogue front end, processor, sensor and antenna. The oscillator which provides the clocks of processing unit, data encoder and decoder [1] is implemented in the analogue front end. By increasing the distance between the tag and the reader, the received power reduces, so the communication with the reader becomes problematic. Therefore in order to increase the reader range, the blocks on the tags should be designed in a way that they dissipate lower power.

According to EPC C1G2 protocol, oscillators designed for RFID tags should have the power consumption in the range of nanowatt and frequency

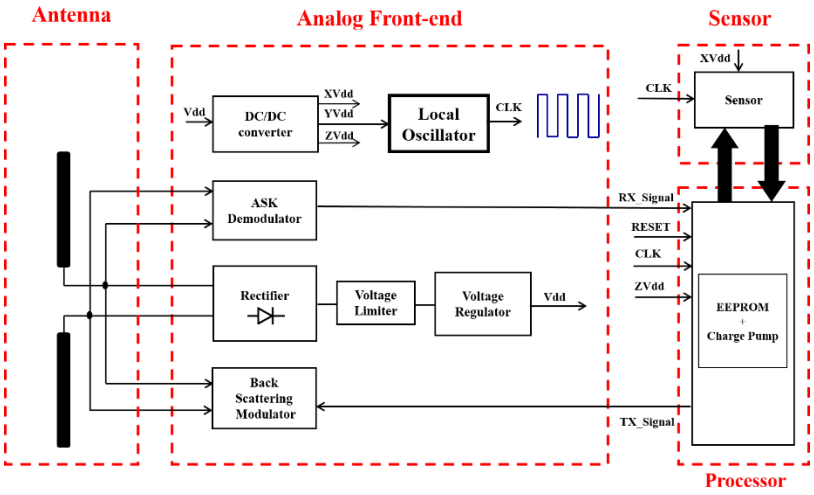

Fig. 1: The block diagram of the passive tag.

deviation of less than 4% [2]. To provide tag clocks in passive tags three constructions are generally used: PLL, RC relaxation and ring oscillator. PLLs usually have low frequency deviation and high power consumption [3], however RC relaxations have low power consumption and high frequency deviation, so they are not desirable to be used in RFID tag chips [4-6]. Single-ended ring oscillators [7, 8] and differential ring oscillators [2, 9] are good choices to be applied in tag designs. The single-ended ring oscillator in which the power consumption is reduced by the method of swing reduction at the inverter stages has been presented by Azarmehr et al. [7]. In addition the low power and high frequency deviation single oscillator has been studied by Cilek et al. [8], and the differential ring oscillator in which deviation is attenuated by the use of temperature compensation circuit has been evaluated by Yin et al. [2]; however its power consumption has been increased.

The phase noise and the jitter value must be alleviated at the oscillator design. Employing high quality factor LC tank is one of the techniques that can improve RF oscillators, however the practical application of them is impossible as a result of the limitation of the space and the integration of circuits in the RFID tags [9, 10].

In this paper, the low power differential ring oscillator which has low frequency deviation to the temperature is designed. Two methods are applied for temperature stability. In the first method the temperature deviation of stage load and in the second method the temperature deviation of differential stage bias current are alleviated. The proposed oscillator architecture as well as the phase noise and power parameters are investigated in section 2, the simulation results are presented in section 3, and finally this paper is concluded in section 4.

2. The designed oscillator

Figure 2 illustrates the proposed oscillator in which the differential delay stages and PMOS transistors are used as the loads of stages. The implementation of a differential delay stage at the oscillator design improves immunity to the common mode noise and provides 50% duty cycle for the output waveform, however due to the high dependency of the threshold voltage and transconductance of MOSFET transistor to the temperature, the frequency of the ring

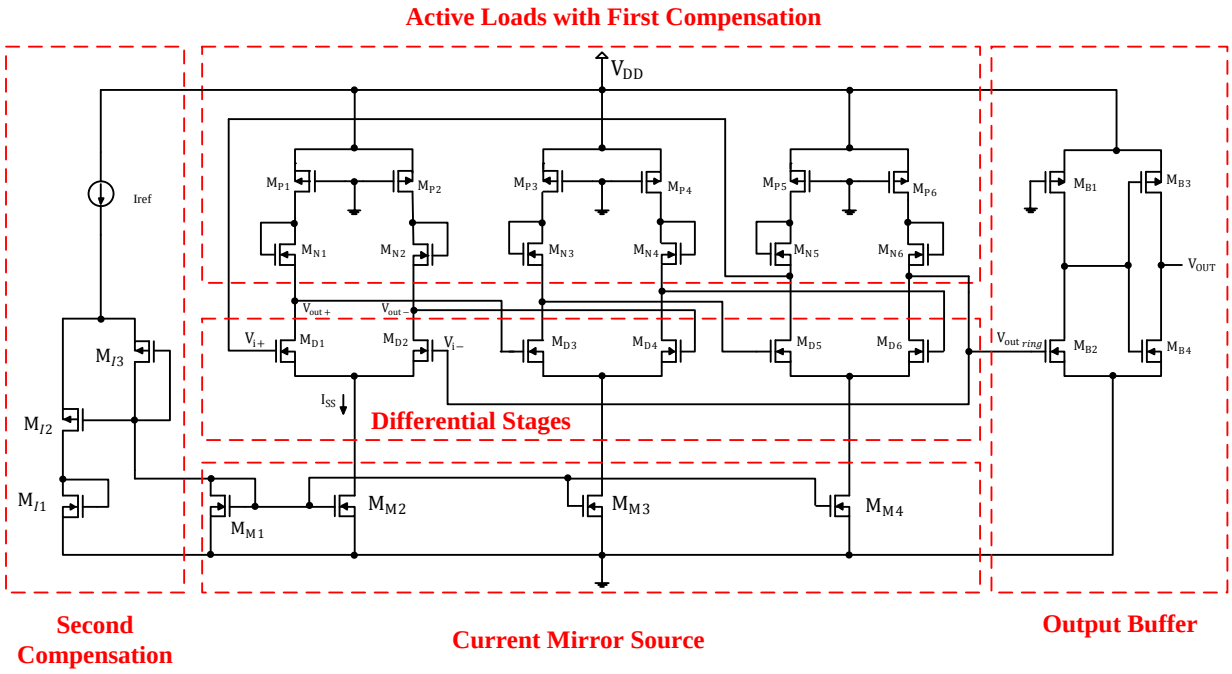

Fig. 2: Designed oscillator circuit.

oscillators using the standard differential stages are not fixed to the temperature variations. To compensate it, various methods such as compensation resistors or operational amplifiers are to be used. Resistors usually have high temperature factor and operational amplifiers make the circuit complicated, so they are used less frequently.

In order to alleviate the dependency of output frequency to temperature, two methods are applied, the temperature compensation via controlling of load temperature variation and temperature compensation via controlling of supply current temperature variation.

2.1. Temperature compensation via controlling of load temperature variation

Regarding to the delay stages intended in differential ring oscillator, to decrease the oscillator frequency temperature sensitivity, output voltage at each stage must become independent of temperature. As shown in Figure 3 two M_P and M_N transistors can be placed at each stage in cascade form due to temperature compensation [11, 12].

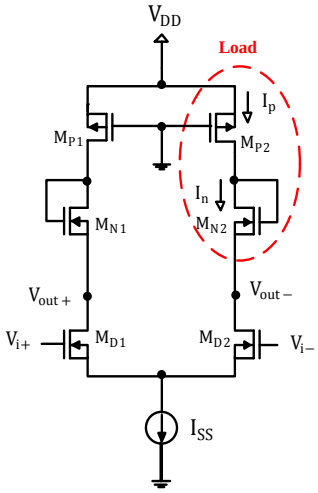

Fig. 3: One stage differential delay by applying temperature compensation load.

In this method by using two load transistors, the swing voltage at each stage will be independent from temperature. PMOS load transistors, M_{P1} and M_{N1} are working at deep triode region and the passing current is calculated by the equation (1). The load NMOS transistors, M_{N1} and M_{N2} work at

subthreshold region and because of V_{dsN1} and $V_{dsN2} \geq 4V_T$, the passing current of them is obtained according to the equation (2).

$$I_{triP} = \mu_P C_{ox} \left(\frac{W}{L}\right)_P \left[(V_{gsP} - V_{thP})V_{dsP}\right] \quad (1)$$

$$I_{subN} = (\eta - 1)\mu_N C_{ox} \left(\frac{W}{L}\right)_N V_T{}^2 exp\left(\frac{V_{gsN} - V_{thN}}{\eta V_T}\right) \quad (2)$$

where η is subthreshold slope, V_{gsN} and V_{gsP} are the gate-source voltages of the NMOS and PMOS transistors, respectively. V_T is the thermal voltage and V_{thP} and V_{thN} are threshold voltages of PMOS and NMOS transistors, respectively.

As a result of the equality of M_N and M_P transistor currents as well as the same temperature behavior of μ_N and μ_P, the equation (3) can be gained.

$$\left(\frac{W}{L}\right)_P \left[(V_{DD} - |V_{thP}|)(V_{DD} - V_{out-} - V_{gsN})\right] = \gamma \left(\frac{W}{L}\right)_N V_T{}^2 exp\left(\frac{V_{gsN} - V_{thN}}{\eta V_T}\right) \quad (3)$$

In this equation γ is $\mu_P/(\eta - 1)\mu_N$. By deriving two sides of equation (3), the result will be the equation (4).

$$\left(\frac{W}{L}\right)_P \left[(V_{DD} - V_{out-} - V_{gsN})\left(-\frac{\partial |V_{thP}|}{\partial T}\right) + (V_{DD} - |V_{thP}|) \times \left(-\frac{\partial V_{out-}}{\partial T}\right)\right] = \gamma \left(\frac{W}{L}\right)_N \left[2V_T \frac{k}{q} + \frac{V_T}{\eta}\left(-\frac{\partial V_{thN}}{\partial T}\right) - \frac{k}{q\eta}(V_{gsN} - V_{thN})\right] exp\left(\frac{V_{gsN} - V_{thN}}{\eta V_T}\right) \quad (4)$$

Output voltage variation with respect to temperature at each stage is gained by the equation (5).

$$\frac{\partial V_{out-}}{\partial T} = \frac{1}{(|V_{thP}| - V_{DD})}\left[\left(\gamma \left(\frac{W}{L}\right)_N \Big/ \left(\frac{W}{L}\right)_P\right)\left[2V_T \frac{k}{q} + \frac{V_T}{\eta}\left(-\frac{\partial V_{thN}}{\partial T}\right) - \frac{k}{q\eta}(V_{gsN} - V_{thN})\right] exp\left(\frac{V_{gsN} - V_{thN}}{\eta V_T}\right) + (V_{DD} - V_{out-} - V_{gsN})\left(\frac{\partial |V_{thP}|}{\partial T}\right)\right] \quad (5)$$

Regarding to equation (5) since $\partial V_{thN}/\partial T$, $\partial |V_{thP}|/\partial T$ and $(V_{gsN} - V_{thN})$ are negative by adjusting the $(W/L)_N$ and $(W/L)_P$ value, V_{out-} deviation with respect to temperature will be zero.

2.2. Temperature compensation via controlling of supply current temperature variation

Considering Figure 2 in order to provide the differential stage current and frequency control, M_{M1}-M_{M4} current mirror transistors are used. If the temperature is increased, V_{th} is decreased, and the bias current of oscillator and so the oscillator frequency will rise.

The temperature coefficient of V_{th} can be compensated by adding M_{I1}-M_{I3} transistors. The increase in temperature results in decrease the threshold voltage and increase the M_{I2} transistor current.

According to equations (6) and (7), since I_{ref} is constant, the passing current of M_{I3} and the passing currents of, respectively, M_{M1}, M_{M2}, M_{M3} and M_{M4} are decreased, therefore increasing the current due to decreasing V_{th} is compensated and the current remains almost constant [1].

$$I_{ref} = I_{I2} + I_{I3} \quad (6)$$

I_{I2} and I_{I3} are respectively the passing current of M_{I2} and M_{I3} transistors. If the seen resistance from drain and source of M_{I3} is supposed to be almost constant with respect to V_{gs} variations, I_{M2} is calculated as follow:

$$I_{M2} = \frac{\left(W/L\right)_{M2}}{\left(W/L\right)_{M1}} \times \frac{V_{gs_{I3}}}{R_{I3}} \quad (7)$$

where $(W/L)_{M2}$ and $(W/L)_{M1}$ is the ratio of W to L in M_{M2} and M_{M1} transistors and R_{I3} is the resistance of M_{I3} in the threshold region, which is calculated by the equation (8).

$$R_{I3}=\frac{\partial V_{ds_{I3}}}{\partial I_{I3}}=\frac{\partial V_{gs_{I3}}}{\partial I_{I3}}=\left[\frac{1}{\eta V_T}\left((\eta-1)\mu_p C_{ox}\left(\frac{W}{L}\right)_{I3}\right.\right.$$
$$\left.\times V_T{}^2 exp\left(\frac{V_{gs_{I3}}-V_{thN}}{\eta V_T}\right)\right)\left(1-exp\left(-\frac{V_{ds_{I3}}}{V_T}\right)\right)+\frac{1}{V_T}$$
$$\times\left((\eta-1)\mu_p C_{ox}\left(\frac{W}{L}\right)_{I3} V_T{}^2 exp\left(\frac{V_{gs_{I3}}-V_{thN}}{\eta V_T}\right)\right)$$
$$\left.\times exp\left(-\frac{V_{ds_{I3}}}{V_T}\right)\right]^{-1}=\left[\frac{1}{\eta V_T}I_{I3}+\frac{1}{V_T}\left((\eta-1)\left(\frac{W}{L}\right)_{I3}\right.\right.$$
$$\left.\left.\times\mu_p C_{ox}V_T{}^2 exp\left(\frac{V_{gs_{I3}}-V_{thN}}{\eta V_T}\right)\right)exp\left(-\frac{V_{ds_{I3}}}{V_T}\right)\right]^{-1} \quad (8)$$

I_{M2} current is obtained in the form of equation (9) by the replacement of the equation (8) in the equation (7). By considering the fact that V_T and I_{I3} are proportional to temperature, according to equation (9) the I_{M2} dependence to temperature is reduced.

$$I_{M2}=\frac{\left(W/L\right)_{M2}}{\left(W/L\right)_{M1}}\times V_{gs_{I3}}\left[\frac{1}{\eta V_T}I_{I3}+\frac{1}{V_T}\left((\eta-1)\left(\frac{W}{L}\right)_{I3}\right.\right.$$
$$\left.\left.\times\mu_p C_{ox}V_T{}^2 exp\left(\frac{V_{gs_{I3}}-V_{thN}}{\eta V_T}\right)\right)exp\left(-\frac{V_{ds_{I3}}}{V_T}\right)\right]$$
(9)

To run processing units and the sensor used in RFID tag, the clock presented by the oscillator must be in rail-to-rail and square form. Also to prevent the influence of the stages on oscillator performance, the buffer implementation will be crucial. The buffer designed for the oscillator is the same as the one shown in Figure 2.

The first stage of the buffer is NMOS amplifier which amplifies the oscillator output signal. The second stage is the inverter which converts the oscillator sinusoidal signal to square signal.

2.3. Power consumption

At N node differential ring oscillator, dynamic power is gained through the equation (10).

$$W_{ring}=\sum_{n=1}^{2N}C_{Ln}V_{DD}^2 f \quad (10)$$

where V_{DD} is the supply voltage, C_{Ln} is the equivalent parasitic capacitance at the inverter output and f is the oscillator central frequency .Also the buffer dynamic power consumption is calculated by equation (11).

$$W_{buffer}=C_{LB}V_{DD}^2 f \quad (11)$$

where C_{LB} is the equivalent parasitic capacitor in the buffer output inverter.

According to Figure 4 the load capacitance (C_L) representing at the first inverter output is gained by the equation (12).

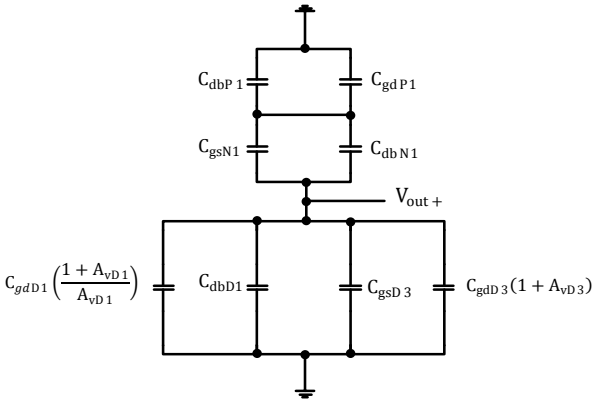

Fig. 4: The equivalent circuit of parasitic capacitor in the first inverter output.

$$C_L=C_{out+}=C_{gdD1}\left(\frac{1+A_{vD1}}{A_{vD1}}\right)+C_{dbD1}+C_{gdD3}\left(1+A_{vD3}\right)$$
$$+C_{gsD3}+\left(\frac{\left(C_{dbN1}+C_{gsN1}\right)\times\left(C_{gdP1}+C_{dbP1}\right)}{\left(C_{dbN1}+C_{gsN1}\right)+\left(C_{gdP1}+C_{dbP1}\right)}\right) \quad (12)$$

where A_{vD1} and A_{vD3} are respectively the differential gains of first and second stages. Similarly C_L is gained in the next inverter outputs. The oscillator output frequency is calculated by the equation (13).

$$f=\frac{2I_D}{N_s C_L V_{swing}} \quad (13)$$

where C_L is seen capacitor from each inverter output, I_D is the current of an inverter stage, V_{swing} is the output voltage swing and N_s is the number of stages.

The buffer output capacitance as seen in Figure 5 is calculated by the equation (14).

$$C_{LB} = C_{out} = 2\left(C_{gdB3} + C_{gdB4}\right) + C_{dbB3} + C_{dbB4} \qquad (14)$$

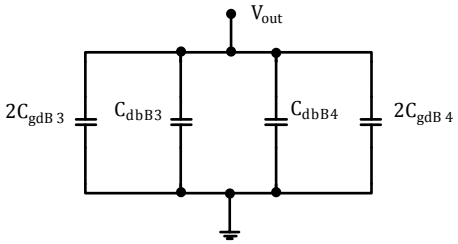

Fig. 5: The equivalent circuit of parasitic capacitor in the buffer output.

By adding W_{buffer} and W_{ring}, the total dynamic power can be calculated.

2.4. The phase noise

Phase noise is undesirable and uncontrolled variations in the oscillator output signal phase which is used for determination of the uncertainty of frequency domain. Phase noise of differential ring oscillator can be calculated based on Dai theory .As shown in [10] phase noise equation for a single-side band is calculated by the equation (15).

$$L\{\Delta\omega\} = \begin{cases} \dfrac{64FkTR}{9V_{pp}^2}\left(\dfrac{\omega_0}{\Delta\omega}\right)^2 & \left(For\, V_{pp} << V_{DD}\right) \\ \dfrac{512FkTRV_{dd}}{27\pi V_{pp}^3}\left(\dfrac{\omega_0}{\Delta\omega}\right)^2 & \left(For\, V_{pp} >> V_{DD}\right) \end{cases} \qquad (15)$$

where : $$V_{pp} = \frac{2\left|dv/dt\right|_{max}}{\omega_0} \qquad (16)$$

where L{Δω} is the single-side band phase noise, F is excess noise factor, R is the equivalent output resistance in the inverter output, |dv/dt| is the maximum slew rate of the output, ω_0 is the central frequency, Δω is the offset from central frequency, K is the Boltzmann constant, and T is the absolute temperature.

3. Simulation results

The proposed oscillator simulated by the cadence software with TSMC 0.18µm CMOS technology. It was done with and without temperature compensation methods. Table 1 illustrates the dimensions of applied transistors.

Table 1: The size of transistors

Transistor	W/L (µm/µm)
M_D	5/0.8
M_P	0.22/4
M_N	3.8/0.2
M_M	5/0.18
M_I	0.4/0.22
M_{B1}	0.22/4
M_{B2} , M_{B4}	0.6/0.18
M_{B3}	1/0.22

Figure 6 shows the frequency versus temperature in the range of -10 to 150°C for the oscillators with and without the application temperature compensation method. Also the oscillator output signal with temperature compensation is shown in Figure 7.

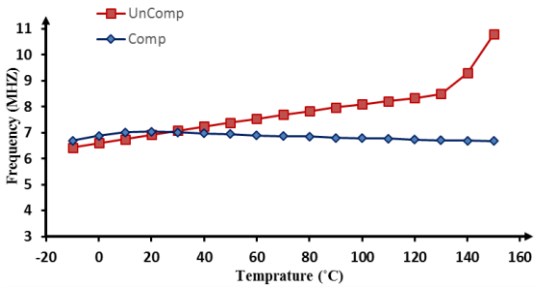

Fig. 6: The oscillator frequency versus temperature with and without the temperature compensation method.

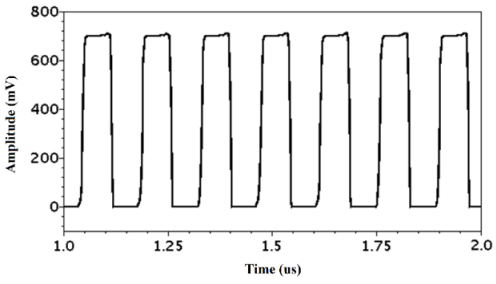

Fig. 7: The output wave form of the simulated oscillator.

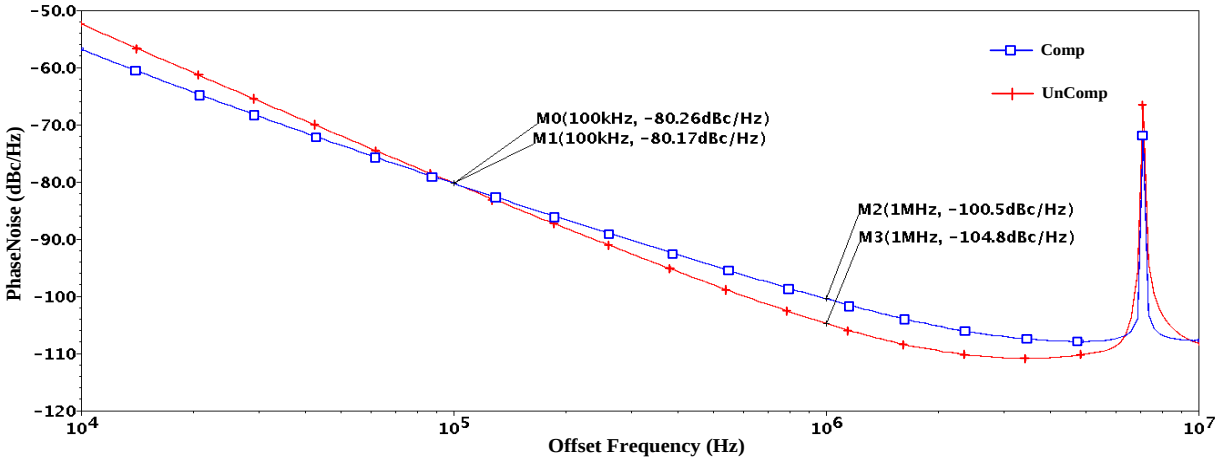

Fig. 8: Phase noise curve of the proposed oscillator.

Figure 8 illustrates the phase noise curve of the simulated oscillator. It is simulated with cadence simulator in 1 MHz and 100 KHz offsets from the central frequency.

As it is clear from Table 2, the noise phase doesn't have any improvements, but the power consumption and the jitter are significantly ameliorated. Based on equation (17) the oscillator frequency deviation without temperature compensation is 3901 ppm/°C in the temperature range of -10 to 150°C while this parameter for the oscillator with temperature compensation is 267 ppm/°C. Also the amount of rms period jitter and rms cycle to cycle jitter in 10000 cycles are 940 ps, and 1640 ps respectively.

$$TC = \frac{\Delta f}{f_0 \times \Delta T} = \frac{f_2 - f_1}{f_0 \times (T_2 - T_1)} \quad (17)$$

Figure 9 shows the mismatch and process variation effects on the output frequency of the oscillator with the Monte Carlo analysis for 500 runs. The mean of output frequency and standard deviation are 6.9 MHz and 338.5 KHz respectively. The layout of the oscillator with temperature compensation is represented in Figure 10, and the occupied area of this oscillator is 29×33μm^2.

Table 2: The comparison between the oscillator with and without temperature compensation

Item	Power Simulation (nW)	Phasenoise (offset 1MHz) Simulation (dBc/Hz)	Phasenoise (offset 1MHz) Calculation (dBc/Hz)	Phasenoise (offset 100KHz) simulation (dBc/Hz)	Phasenoise (offset 100KHz) Calculation (dBc/Hz)	Jitter rms (10K cycle) (ps)	Jitter rms (cycle to cycle) (ps)	TC (ppm/◦C)	Variation (%)
without temperature compensation	648	-104.8	-111.7	-80.1	-89.4	2015	3492	3901 (-10 _ 150 ℃)	64
with temperature compensation	502	-100.4	-107.2	-80.2	-87.3	940	1640	267 (-10 _ 150 ℃)	4.1

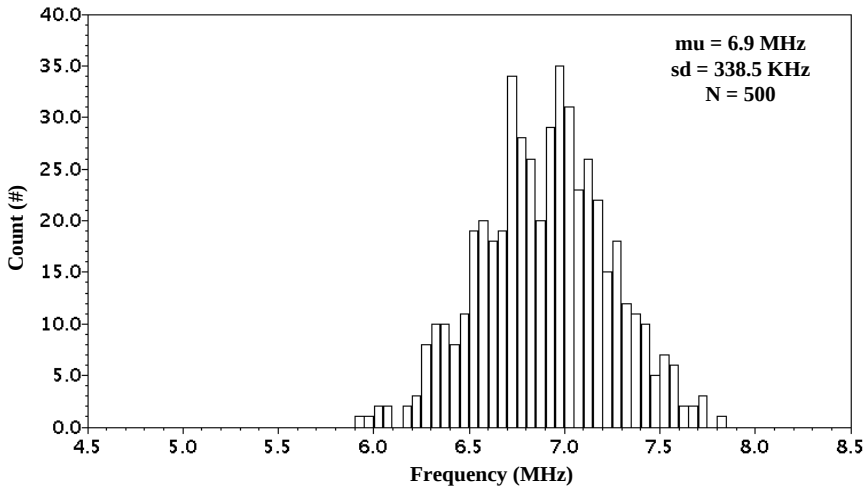

Fig. 9: The result of the Monte carlo analysis for the proposed oscillator.

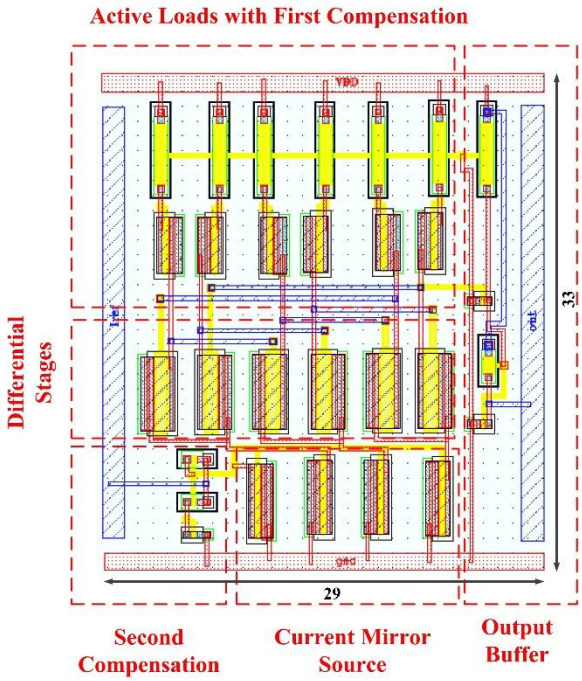

Fig. 10: The proposed oscillator layout.

Table 3 illustrates the comparison between the proposed oscillator and the other oscillators. It shows that the size of the proposed oscillator is smaller also it uses much less power and jitter while its output frequency deviation in the temperature range of -10 to 150°C is so little. In addition, the phase noise performance in 100 KHz offset, compared to other oscillators, is more desirable.

Table 3: The comparison between the proposed oscillator and the other oscillators

Ref	Tech (nm)	Type	VDD (V)	Freq (MHz)	Power (µw)	Phasenoise /jitter (dBc/Hz) / (ns)	Range Temp(◦C)	TC (ppm/◦C)	Variation (%)	Area (μm^2)
[1]	180	Single-ended Ring	1	8	0.725	------	0 _ 50	250	1.25	550
[2]	180	Differential Ring	1	2.17	1.5	------	-40 _ 80	225	2.7	------
[3]	180	Single-ended Ring	1	2.56	2	------	-15 _ 75	356	3.2	221400
[5]	180	Relaxation	1.8	14	43.3	-90 (100KHz offset) 2.8 (1.5K cycles)	-40 _ 125	46	0.75	40000
[9]	350	Differential Ring	3.3	922	6600	-116 (10MHz offset)	------	------	------	314900
[13]	130	Single-ended Ring	0.7	3	0.24	------	0 _ 100	660	6.6	------
This work	180	Differential Ring	0.7	7	0.502	-80.2(100KHz offset) 0.94 (10K cycles)	-10 _ 150	267	4.1	957

4. Conclusions

This paper is proposed CMOS differential ring oscillator with 502 nW power consumption in which by applying temperature compensation, the temperature coefficient of the oscillator in the temperature range of -10 to 150°C and the central frequency of 7 MHz is 267 ppm/ºC. The phase noise of the proposed oscillator at 100 KHz offset frequency is -80.2 dBc/Hz. In this proposed oscillator the jitter period for the 10000 cycles is 0.94 ns (rms).

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